CLAIM AMENDMENTS

Please cancel, without prejudice, 1-51, as indicated on the following listing of all the claims in the present application after this Amendment:

1-51. (Canceled)

52.(Previously Presented) A circuit for pixel interpolation, the circuit comprising:

a plurality of downscale circuits, each downscale circuit coupled to receive one or more sets of field pixels of a video signal, and each downscale circuit operable to generate one or more downscaled field pixels from the one or more sets of field pixels;

a plurality of edge detector circuits, each edge detector circuit coupled to receive one or more downscaled field pixels from a respective downscale circuit and operable to detect corresponding edges therefrom;

a field pixel slope determinator coupled to received the output of the plurality of edge detection circuits and determine field pixel slopes therefrom;

an interpolated pixel slope determinator coupled to receive the field pixel slopes and determine an interpolated pixel slope therefrom; and

an interpolated pixel generator coupled to receive the interpolated pixel slope and generate an interpolated pixel based thereupon.

53.(Previously Presented) The circuit of Claim 52, wherein said video signal is an interlaced video signal.

54.(Previously Presented) The circuit of Claim 52 wherein the one or more sets of field pixels include a first set of field pixels, the first set of field pixels including field pixels from a field line having the first field pixel.

55.(Previously Presented) The circuit of Claim 52 wherein the one or more sets of field pixels include a second set of field pixels, the second set of field pixels including field pixels from a field line above a field line having the first field pixel.

56.(Previously Presented) The circuit of Claim 52 wherein the one or more sets of field pixels include a third set of field pixels, the third set of field pixels including field pixels from a field line below a field line having the first field pixel.

57.(Previously Presented) The circuit of Claim 52 wherein each downscale circuit averages a first set of field pixels, the first set of field pixels including at least 3 field pixels from a field line having the first field pixel.

58.(Previously Presented) The circuit of Claim 52 wherein each downscale circuit averages a second set of field pixels, the second set of field pixels including at least 3 field pixels from a field line above a field line having the first field pixel.

59.(Previously Presented) The circuit of Claim 52 wherein each downscale circuit averages a third set of field pixels, the third set of field pixels including at least 3 field pixels from a field line below a field line having the first field pixel.

60.(Previously Presented) The circuit of Claim 52 wherein each downscale circuit low-pass filters a first set of field pixels, the first set of field pixels including at least 3 field pixels from a field line having the first field pixel.

61.(Previously Presented) The circuit of Claim 52 wherein each downscale circuit low-pass filters a second set of field pixels, the second set of field pixels including at least 3 field pixels from a field line above a field line having the first field pixel.

62.(Previously Presented) The circuit of Claim 52 wherein each downscale circuit low-pass filters a third set of field pixels, the third set of field pixels including at least 3 field pixels from a field line below a field line having the first field pixel.

63.(Previously Presented) The circuit of Claim 52 wherein each edge detector circuit includes a high-pass filter.

64.(Previously Presented) The circuit of Claim 52 wherein each edge detector circuit includes a [-1/4, 1/2, -1/4] high pass filter.